Listing of the Claims:

The office action notes that the substitute specification was not entered in the case and that the claims provided in the substitute specification were not entered in the case. However, this office action does not agree with the USPTO's own records which show in the published application 2007/0138580 all of the claims that were presented with the substitute specification document. Based on the Examiners statements and requirements, and the objection to claims 21, and 27-30, the applicant assumes that the Examiner has conducted the Examination based on the translation document provided with the application, and not on the amended claims, as they were amended during the international stage of prosecution. The undersigned hereby provisionally requests that the claims examined by the Examiner be amended as filed; however, should the Examiner reverse his position on the official record for this case, the Examiner is requested to examine the claims pending in U.S. Patent Publication 2007/0138580 without any amendment.

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1. (Canceled)

2. (Currently amended) The semiconductor device as set forth in claim 32 ~~1~~, wherein said electrically insulating film contains one of Hf and Zr.

3. (Currently amended) The semiconductor device as set forth in claim 32 ~~1~~, further comprising a layer containing one of Hf and Zr therein between said electrically insulating film and said gate electrode.

4. (Currently amended) The semiconductor device as set forth in claim 32~~1~~, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and one of a Hf-containing layer and a Zr-containing layer.

5. (Currently amended) The semiconductor device as set forth in claim 32 ~~1~~,

wherein said electrically insulating film contains HfSiON.

6. (Currently amended) The semiconductor device as set forth in claim 32 ~~1~~, further comprising a HfSiON layer between said electrically insulating film and said gate electrode.

7. (Currently amended) The semiconductor device as set forth in claim 32 ~~1~~, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and a HfSiON layer.

8-9. (Canceled)

10. (Currently amended) The semiconductor device as set forth in claim 32 ~~9~~, wherein, said gate electrode contains nickel silicide as a primary constituent, and assuming that a region of said nickel silicide (including nickel (Ni) as said metal M) making contact with said gate insulating film is expressed with NixSi1-X ($0<X<1$), said X is equal to or greater than 0.6 and smaller than 1 ($0.6 \leq X<1$) in said nickel silicide contained in a gate electrode formed above a p-channel, and said X is greater than 0 and equal to or smaller than 0.5 ($0<X \leq 0.5$) in said nickel silicide contained in a gate electrode formed above a n-channel.

11. (Currently amended) The semiconductor device as set forth in claim 32 ~~9~~, wherein said nickel silicide contained in said gate electrode formed above said p-channel contains Ni3Si phase as a principal constituent at least in a region through which said nickel silicide makes contact with said gate insulating film, and said nickel silicide contained in said gate electrode formed above said n-channel contains one of NiSi phase and NiSi2 phase as a principal constituent at least in a region through which said nickel silicide makes contact with said gate insulating film.

12. (Currently amended) A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film,

~~characterized in that~~ wherein at least a region of said gate electrode making contact with said gate insulating film is composed of silicide containing Ni_3Si phase as a principal constituent.

13. (Original) The semiconductor device as set forth in claim 12, wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

14. (Original) The semiconductor device as set forth in claim 13, wherein said electrically insulating film contains one of Hf and Zr.

15. (Original) The semiconductor device as set forth in claim 13, further comprising a layer containing one of Hf and Zr therein between said electrically insulating film and said gate electrode.

16. (Original) The semiconductor device as set forth in claim 13, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and one of a Hf-containing layer and a Zr-containing layer.

17. (Original) The semiconductor device as set forth in claim13, wherein said electrically insulating film contains HfSiON.

18. (Original) The semiconductor device as set forth in claim 13, further comprising a HfSiON layer between said electrically insulating film and said gate electrode.

19. (Original) The semiconductor device as set forth in claim 13, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and a HfSiON layer.

20. (Currently amended) The semiconductor device as set forth in claim 12 ~~any~~

~~one of claims 12 to 19~~, wherein said gate electrode is included in a p-type MOSFET.

21. (Currently amended) A method of fabricating a semiconductor device ~~defined in any one of claims 1 to 9~~, comprising:

depositing poly-silicon (poly-Si) on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

depositing one of metals selected from Ni, Pt, Ta, Ti, Hf, Co, Zr and V ~~metal M~~ on said gate electrode;

thermally annealing said gate electrode and said one of metals ~~metal M~~ to entirely turn said gate electrode to silicide of said one of metals ~~metal M~~; and

removing a portion of said one of metals ~~metal M~~ which was not turned into said silicide, by etching,

assuming that said one of metals is expressed with M, and said silicide has a portion through which said silicide makes contact with said gate insulating film and which has a composition expressed with M_xSi_{1-x} ($0<X<1$),

wherein said metal M has such a thickness t1 above a p-channel device that, when poly-silicon and said metal M react with each other to make silicide, a portion of said silicide making contact with said gate insulating film has composition expressed with M_xSi_{1-x} ($0.5<X<1$), and has such a thickness t2 above a n-channel device that, when poly-silicon and said metal M react with each other to make silicide, a portion of said silicide making contact with said gate insulating film has composition expressed with M_xSi_{1-x} ($0<X\leq 0.5$).

22. (Currently amended) A method of fabricating a semiconductor device ~~defined in claim 10~~, comprising:

depositing poly-silicon on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

forming a nickel (Ni) film on said gate electrode;

thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode to nickel silicide (NiSi); and

removing a portion of said nickel film which was not turned into said nickel silicide, by etching,

wherein said nickel film has such a thickness t1 above a p-channel device that, when poly-silicon and nickel react with each other to make nickel silicide, a portion of said nickel silicide making contact with said gate insulating film has composition expressed with Ni_xSi_{1-x} ($0.6 \leq X < 1$), and has such a thickness t2 above a n-channel device that, when poly-silicon and nickel react with each other to make nickel silicide, a portion of said nickel silicide making contact with said gate insulating film has composition expressed with Ni_xSi_{1-x} ($0 < X \leq 0.5$).

23. (Currently amended) A method of fabricating a semiconductor device ~~defined in claim 11~~, comprising:

depositing poly-silicon on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

forming a nickel (Ni) film on said gate electrode;

thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode to nickel silicide (NiSi); and

removing a portion of said nickel film which was not turned into said nickel silicide, by etching,

wherein said nickel film has such a thickness t1 above a p-channel device that, when poly-silicon and nickel react with each other to make nickel silicide, said nickel silicide has Ni_3Si phase as a principal constituent, and has such a thickness t2 above a n-channel device that, when poly-silicon and nickel react with each other to make nickel silicide, said nickel silicide has one of NiSi phase and $NiSi_2$ phase as a principal constituent.

24. (Original) The method as set forth in claim 23, wherein a ratio of a thickness TNi of said nickel film to a thickness TSi of said poly-silicon is defined as $TNi/TSi \geq 1.60$ to form said gate electrode including Ni_3Si phase as a principal constituent.

25. (Original) The method as set forth in claim 23, wherein a ratio of a thickness TNi of said nickel film to a thickness TSi of said poly-silicon is defined as $0.55 \leq TNi/TSi \leq 0.95$ to form said gate electrode including NiSi phase as a principal constituent.

26. (Original) The method as set forth in claim 23, wherein a ratio of a thickness TNi of said nickel film to a thickness TSi of said poly-silicon is defined as $0.28 \leq TNi/TSi \leq 0.54$, and said gate electrode and said nickel film are thermally annealed at 650 degrees centigrade or higher to form said gate electrode including $NiSi_2$ phase as a principal constituent.

27. (Currently amended) The method as set forth in claim 26 ~~any one of claims 21 to 23~~, wherein the step of depositing said metal M or forming said nickel film comprises:

after forming said metal M or said nickel film above a n-channel device or a p-channel device by the thickness of t2, forming diffusion-preventing layer which is stable to said metal M or nickel, only above said n-channel device; and

depositing said metal M or forming said nickel film by the thickness of (t1 - t2).

28. (Original) The method as set forth in claim 27, wherein said diffusion-preventing layer can be etched in selected areas relative to silicide of said metal M.

29. (Original) The method as set forth in claim 27, wherein said diffusion-preventing layer contains one of TiN and TaN as a primary constituent.

30. (Currently amended) The method as set forth in claim 26 ~~any one of claims 21 to 29~~, wherein said gate electrode and said metal M or said nickel film are thermally annealed for silicidation at such a temperature that a resistance of metal silicide formed in a diffusion contact region of said semiconductor device is not increased.

31. (Currently amended) A method of fabricating a semiconductor device ~~defined in claim 10~~, comprising:

depositing poly-silicon on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

forming a nickel (Ni) film on said gate electrode;

thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode to nickel silicide (NiSi); and

removing a portion of said nickel film which was not turned into said nickel silicide, by etching,

wherein a ratio of a thickness TNi of said nickel film to a thickness TSi of said poly-silicon is defined as $1.60 \leq Tni/TSi$.

32. (New) A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film, in this order,

wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

said gate electrode contains nickel silicide as a primary constituent, and has a region through which said gate electrode makes contact with said gate insulating film and which has a composition expressed with Ni_xSi_{1-x} ($0<X<1$), and

said X is greater than 0.5 ($X>0.5$) in said nickel silicide contained in a gate electrode formed above a p-channel, and said X is equal to or smaller than 0.5 ($X\leq 0.5$) in said nickel silicide contained in a gate electrode formed above a n-channel.

33. (New) A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film, in this order,

wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

said gate electrode contains platinum silicide as a primary constituent, and has a region through which said gate electrode makes contact with said gate insulating film and which has a composition expressed with Pt_xSi_{1-x} ($0<X<1$), and

said X is greater than 0.5 ($X>0.5$) in said platinum silicide contained in a gate electrode formed above a p-channel, and said X is equal to or smaller than 0.5 ($X\leq 0.5$) in said platinum silicide contained in a gate electrode formed above a

n-channel.

34. (New) A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film, in this order,

wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

said gate electrode contains tantalum silicide as a primary constituent, and has a region through which said gate electrode makes contact with said gate insulating film and which has a composition expressed with Ta_xSi_{1-x} ($0<X<1$), and

said X is greater than 0.5 ($X>0.5$) in said tantalum silicide contained in a gate electrode formed above a p-channel, and said X is equal to or smaller than 0.5 ($X\leq 0.5$) in said tantalum silicide contained in a gate electrode formed above a n-channel.

35. (New) A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film, in this order,

wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

said gate electrode contains titanium silicide as a primary constituent, and has a region through which said gate electrode makes contact with said gate insulating film and which has a composition expressed with Ti_xSi_{1-x} ($0<X<1$), and

said X is greater than 0.5 ($X>0.5$) in said titanium silicide contained in a gate electrode formed above a p-channel, and said X is equal to or smaller than 0.5 ($X\leq 0.5$) in said titanium silicide contained in a gate electrode formed above a n-channel.

36. (New) A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film, in this order,

wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

said gate electrode contains hafnium silicide as a primary constituent, and has a region through which said gate electrode makes contact with said gate insulating film and which has a composition expressed with Hf_xSi_{1-x} ($0<X<1$), and

said X is greater than 0.5 ($X>0.5$) in said hafnium silicide contained in a gate electrode formed above a p-channel, and said X is equal to or smaller than 0.5 ($X\leq 0.5$) in said hafnium silicide contained in a gate electrode formed above a n-channel.

37. (New) A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film, in this order,

wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

said gate electrode contains cobalt silicide as a primary constituent, and has a region through which said gate electrode makes contact with said gate insulating film and which has a composition expressed with Co_xSi_{1-x}($0<X<1$), and

said X is greater than 0.5 ($X>0.5$) in said cobalt silicide contained in a gate electrode formed above a p-channel, and said X is equal to or smaller than 0.5 ($X\leq 0.5$) in said cobalt silicide contained in a gate electrode formed above a n-channel.

38. (New) A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film, in this order,

wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

said gate electrode contains zirconium silicide as a primary constituent, and has a region through which said gate electrode makes contact with said gate

insulating film and which has a composition expressed with Zr_xSi_{1-x} ($0<X<1$), and

said X is greater than 0.5 ($X>0.5$) in said zirconium silicide contained in a gate electrode formed above a p-channel, and said X is equal to or smaller than 0.5 ($X \leq 0.5$) in said cobalt zirconium contained in a gate electrode formed above a n-channel.

39. (New) A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film, in this order,

wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

said gate electrode contains vanadium silicide as a primary constituent, and has a region through which said gate electrode makes contact with said gate insulating film and which has a composition expressed with V_xSi_{1-x} ($0<X<1$), and

said X is greater than 0.5 ($X>0.5$) in said vanadium silicide contained in a gate electrode formed above a p-channel, and said X is equal to or smaller than 0.5 ($X \leq 0.5$) in said cobalt vanadium contained in a gate electrode formed above a n-channel.